REMARKS

In order to avoid additional filing fees, independent Claims 14 and 23, which have been withdrawn from consideration, are being cancelled without prejudice to applicant's right to pursue them in one or more divisional applications.

The objection to the drawings is not understood. Support for the "source diffusion in the active area directly beneath the select gate at a second end of each row" is found in the embodiment of Figure 7 where source region 51 is directly beneath select gate 45 at the right end of the row of gates. The Examiner appears to have overlooked that embodiment in making the objection, and applicant trusts that the objection will be withdrawn.

The claims are being amended in a manner which should overcome the Examiner's objections regarding the manner in which the stacked gates are claimed and the use of relative terminology which might prevent one from ascertaining the scope of the invention. However, in a number of instances, the relative terms are perfectly proper, and they have not been deleted. For example, where a claim calls for a relatively thin oxide and a relatively thick oxide, a person skilled in the art is going to know that the claim simply requires the second oxide to be thicker than the first. Likewise, a claim calling for a relatively low voltage and a relatively high voltage simply requires the second voltage to be higher than the first. With this clarification and the amendments which are being made, applicant trusts that the objections will be withdrawn.

Claims 1 - 13 and 15 - 22 have all been rejected under 35 U.S.C. §102 as being anticipated by Noda (U.S. 6,400,604). Reconsideration and withdrawal of that rejection is requested.

Initially, it should be pointed out that the rejection is improper because the device shown in Noda is not a NAND gate, as claimed, but rather a matrix of single memory cell units each having a memory cell MC with a select gate SG1, SG2 on either side of it (Col. 5, lines 1 - 10).

Moreover, there is another fundamental and significant structural difference between applicant's invention and the device shown in Noda. In that regard, it will be noted that Noda has drain and source diffusion regions 38 between the memory cells

and the select gates on either side of them. In contrast, in applicant's invention, a plurality of stacked gates 36 and select gates 43, 44, 45 are arranged in a row between bit line diffusion 50 and source region 51 with no other diffusions between them. As can be seen by comparing Figures 4 and 8 of applicant's specification with Figure 3 of Noda, without the intervening diffusions, the stacked gates and the select gates can be positioned much closer together, which results in a much higher gate density in a given chip area. The claims are being amended to emphasize this important difference.

As amended, Claim 1 distinguishes from Noda in calling for a substrate having an active area, a bit line diffusion and a source region in the active area with no other diffusions in the active area between the bit line diffusion and the source region, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source region, with each of the stacked gates having a control gate positioned above a floating gate and the last select gate in the row at least partially overlapping the source region, a bit line above the row, a bit line diffusion in the active area toward a first end of each row, and a bit line contact interconnecting the bit line and the bit line diffusion.

Claims 2 - 13 depend from Claim 1 and distinguish over Noda for the same reasons as their amended parent claim. In addition, they call for additional features and elements which are not found in Noda.

Claim 2, for example, specifies that the stacked gates and the select gates are self-aligned relative to each other. Contrary to the Examiner's suggestion, the portion of Noda cited by him (Col. 6, lines 48 - 51) does not teach that relationship.

Claim 3 further distinguishes in calling for a relatively thin tunnel oxide between the floating gates and the substrate, a first relatively thick dielectric between the floating gates and the select gates, and a second relatively thick dielectric between floating gates and control gates. That relationship is not found in Noda where the tunnel insulating film 34 is shown as being the same thickness as the insulating film 36 above the floating gate 35 in Figure 4a and thicker in Figure 4b.

Claim 4, as amended, specifies that the control gates and the select gates surround the floating gates in a manner which provides an inter-gate capacitance which is large enough for voltage coupling between the gates during program and erase operations. Notwithstanding the Examiner's speculation about "implied" capacitance

in Noda, the reference itself is devoid of any teaching of an inter-gate capacitance which is large enough to provide voltage coupling between the gates during program and erase operations.

Claim 5 specifies that erase paths extend from the floating gates, through tunnel oxides below the floating gates to channel regions in the substrate, and further distinguishes over Noda in specifying that voltage is coupled to the floating gates both from the control gates and from the select gates. The portion of Noda cited by the Examiner (Col. 9, lines 37 - 50) says absolutely nothing about voltages being coupled to the floating gates from the control gates and select gates, and the argument the Examiner makes about a thin tunnel oxide not reducing the voltage in the floating gate is irrelevant.

Claim 6 specifies that program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and further specifies that voltage is coupled to the floating gates both from the control gates and from the select gates on the sides of the stacked gates toward the source region. In explaining the rejection of this claim, the Examiner first argues that the specified programming paths exist in Noda because "channel regions" 38 are highly doped and, hence, conductive. However, what the Examiner calls channel regions are actually drain and source regions, and there is no mention whatsoever in Noda of program paths which extend in the manner specified. In explaining this rejection, the Examiner also repeats the same specious arguments about coupled voltages and a thin tunnel oxide that he made in connection with the rejection Claim 5.

Claim 7 further distinguishes over Noda in specifying that program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and the select gate on the bit line side of the stacked gates in a selected cell is biased at a lower voltage than the other select gates in the row to control channel current for efficient hot carrier injection during a program operation. In rejecting this claim, the Examiner makes the same erroneous argument about the program paths that he made in connection with Claim 6, then he tries to ignore the remainder of the claim on the basis that it is functional or intended use. The language in question specifies that the select gate on the bit line side of the stacked gates in a selected cell is biased at a lower voltage than the other select gates in the row to control channel current for

efficient hot carrier injection during a program operation. Contrary to the Examiner's contention, the biasing of a specific element in a specific manner relative to other specific elements in a specific operational mode is indeed a structural limitation. Even assuming that the Examiner is correct in his speculation that the claimed voltages can be imparted in Noda because the select gates are independent of each other, that does not anticipate the invention as claimed because Noda itself does not teach the application of such voltages.

Claim 8 further distinguishes over Noda in specifying that the select gates in unselected cells are biased at a voltage to turn on the channels beneath them to form a conduction path between the bit line diffusion and the source region. In rejecting this claim, the Examiner first argues that the select gates in unselected cells ***can*** be biased in the manner claimed, then argues that the limitation has no patentable weight because it is intended use or functional. The first half of the argument is fallacious because the individual cell unit structure shown in Noda does not have a bit line diffusion and a source region at opposite ends of a row of gates between which a conduction path can be formed. Moreover, the portion of Noda cited by the Examiner in support of the rejection (Col. 6, lines 63 - 67) says nothing whatsoever either about biasing select gates in unselected cells or about forming a conduction path between a bit diffusion and a source region at opposite ends of a row of gates. The intended use or functional language argument is the same one that the Examiner made in connection with the rejection of Claim 7, and it is fallacious for the same reasons.

Claim 9 further distinguishes over Noda in specifying that the bit line for a row containing a selected cell to be programmed is held at 0 volts, a relatively low positive voltage is applied to a cell select gate for the selected cell, a relatively high positive voltage is applied to the source region at the end of the row in which the selected cell is located, a relatively high positive voltage is applied to the control gate in the selected cell, a relatively high positive voltage is applied to the select gates for unselected cells, and a relatively high positive voltage is applied to the control gates in the unselected cells. In rejecting this claim, the Examiner once again makes the fallacious argument about voltages which "can" be applied to different elements, rather than what is actually taught by Noda. In so doing, he is applying voltages to elements which do not even exist in Noda, such as the source diffusion at the end of the row. As discussed above,

limitations calling for the application of specific voltages are structural limitations, not intended use, and they cannot be ignored, as the Examiner has tried to do.

Claim 10 further distinguishes over Noda in specifying that an erase path is formed by a relatively high negative voltage on the control gates and a relatively low negative voltage on the select gates, with the bit line diffusion, the source region and the P-well at 0 volts. In rejecting this claim, the Examiner once again makes the fallacious arguments about voltages which "can" be applied to different elements, rather than what is actually taught by Noda, and about such limitations having no patentable weight because the are intended use or functional. As discussed above, limitations calling for the application of specific voltages are structural limitations, not intended use, and they cannot be ignored, as the Examiner has tried to do.

Claim 11 further distinguishes over Noda in specifying that an erase path is formed by a relatively high negative voltage on the control gates, and relatively low negative voltage on the select gates, with the active area at a positive voltage and the bit line diffusion and the source region floating. In rejecting this claim, the Examiner once again makes the fallacious arguments about voltages which "can" be applied to different elements, rather than what is actually taught by Noda, and about such limitations having no patentable weight because the are intended use or functional. Noda itself says nothing about the formation of an erase path by a relatively high negative voltage on control gates and a relatively low negative voltage on select gates, with an active area at a positive voltage and the bit line diffusion and the source region floating. As discussed above, limitations calling for the application of specific voltages are structural limitations, not intended use, and they cannot be ignored, as the Examiner has tried to do.

Claim 12 further distinguishes over Noda in specifying that a read path is formed by turning on the select transistors and the stacked control and floating gate transistors in unselected cells, with the common source at 0 volts, the bit line diffusion at 1 - 3 volts, and the control gate of the selected cell biased at 0 – 1.5 volts to form a conduction channel under the floating gate for an erase state and a non-conduction channel for a program state. In rejecting this claim, the Examiner once again makes the fallacious arguments about voltages which "can" be applied to different elements, rather than what is actually taught by Noda, and about such limitations having no

patentable weight because the are intended use or functional. Noda itself says nothing about the formation of a read path by turning on the select transistors and the stacked control and floating gate transistors in unselected cells, with the common source at 0 volts, the bit line diffusion at 1 - 3 volts, and the control gate of the selected cell biased at 0 – 1.5 volts to form a conduction channel under the floating gate for an erase state and a non-conduction channel for a program state. As discussed above, limitations calling for the application of specific voltages are structural limitations, not intended use, and they cannot be ignored, as the Examiner has tried to do.

Claim 13 further distinguishes over Noda in calling for an erase path which can erase the whole cell array simultaneously and a program path which is single cell selectable. In rejecting this claim, the Examiner makes a wholly unsupported argument that an erase path and a program path which function as claimed "can" be created "through appropriate biasing." This overlooks the simple fact that such paths are not found in Noda itself. The Examiner then goes on to argue that it doesn't matter anyway because claim language relating to application of voltage is functional or directed to intended use. That, of course, totally misses the mark because there is no language about the application of voltages in Claim 13. The claim simply calls for an erase path which can erase the whole cell array simultaneously and a program path which is single cell selectable.

Independent Claim 15, as amended, distinguishes over Noda in calling for a substrate having an active area, a bit line diffusion and a source diffusion in the active area with no other diffusions in the active area between the bit line diffusion and the source diffusion, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source diffusion, with each of the stacked gates having a control gate positioned above a floating gate and the last select gate in the row being directly above the source diffusion, a bit line above the row, and a bit line contact interconnecting the bit line and the bit line diffusion.

Claims 16 - 18 depend from Claim 15 and are directed to patentable subject matter for the same reasons as their amended parent claim. In addition, they call for additional features and elements which are not found in Noda.

Claim 16, for example, further distinguishes over Noda in specifying that the select gates are self-aligned to the control and floating gates. As pointed out above in

connection with Claim 2, the portion of Noda cited by the Examiner (Col. 6, lines 48 - 51) does not teach that relationship.

Claim 17 further distinguishes over Noda in calling for a relatively thin tunnel oxide between the floating gates and the substrate, a first relatively thick dielectric between the floating gates and the select gates, and a second relatively thick dielectric between floating gates and control gates. As pointed out above in connection with Claim 3, that relationship is not found in Noda where the tunnel insulating film 34 is shown as being the same thickness as the insulating film 36 above the floating gate 35 in Figure 4a and thicker in Figure 4b.

Claim 18 further distinguishes over Noda in specifying that the control gates and the select gates surround the floating gates in a manner which provides a relatively large inter-gate capacitance which is large enough for voltage coupling between the gates during program and erase operations. As discussed above in connection with Claim 4, notwithstanding the Examiner's speculation about "implied" capacitance in Noda, the reference itself is devoid of any teaching of an inter-gate capacitance which is large enough to provide voltage coupling between the gates during program and erase operations.

Independent Claim 19, as amended, distinguishes over Noda in calling for a substrate having an active area, bit line diffusions and source diffusions spaced alternately in the active area with no other diffusions between them, a plurality of stacked gates and select gates arranged alternately in rows, with each of the stacked gates having a control gate positioned above a floating gate and the last select gates in each of the rows at least partially overlapping the source diffusions between the rows, a bit line above each row, and bit line contacts interconnecting the bit lines and the bit line diffusions.

Claims 20 - 22 depend from Claim 19 and are directed to patentable subject matter for the same reasons as their amended parent claim. In addition, they call for additional features and elements which are not found in Noda.

Claim 20, for example, further distinguishes over Noda in specifying that the floating gate and the control gate in each of the stacked gates are self-aligned with respect to each other. As pointed out above in connection with Claims 2 and 16, the

portion of Noda cited by the Examiner (Col. 6, lines 48 - 51) does not teach that relationship.

Claim 21 further distinguishes in calling for a relatively thin tunnel oxide between the floating gates and the substrate, a first relatively thick dielectric between the floating gates and the select gates, and a second relatively thick dielectric between floating gates and control gates. As pointed out above in connection with Claims 3 and 17, that relationship is not found in Noda where the tunnel insulating film 34 is shown as being the same thickness as the insulating film 36 above the floating gate 35 in Figure 4a and thicker in Figure 4b.

Claim 22 further distinguishes over Noda in specifying that the control gates and the select gates surround the floating gates in a manner which provides an inter-gate capacitance which is large enough for voltage coupling between the gates during program and erase operations. As discussed above in connection with Claims 4 and 18, notwithstanding the Examiner's speculation about "implied" capacitance in Noda, the reference itself is devoid of any teaching of an inter-gate capacitance which is large enough to provide voltage coupling between the gates during program and erase operations.

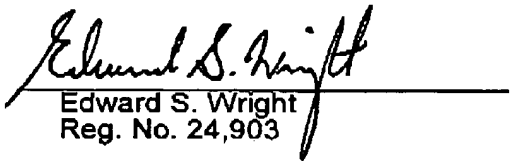
In order to more fully round out the protection to which applicant is believed to be entitled a new Claim 24 is being added. That claim distinguishes over Noda in calling for A NAND flash memory cell array, comprising: a substrate having an active area, a bit line diffusion and a source region in the active area with no other diffusions in the active area between the bit line diffusion and the source region, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source region, with each of the stacked gates having a control gate and a floating gate with self-aligned sides adjacent to the select gates, erase paths between the floating gates and channel regions in the active area beneath the stacked gates, and voltage coupling from the control gates and the select gates to the floating gates. A NAND gate having these elements is not even remotely suggested by Noda.

With this amendment, it is respectfully submitted that Claims 1 - 13, 15 - 22, and 24 are all directed to patentable subject matter and that the application is in condition for allowance.

To avoid unnecessary additional filing fees, independent Claims 14 and 23, which have been withdrawn from consideration, are being cancelled without prejudice to applicant's right to pursue them in one or more divisional applications.

The Commissioner is authorized to charge any fees required in this matter, including extension fees, to Deposit Account 50-2975, Docket No. A-75000.

Respectfully submitted,



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